An application specific integrated for multi anode PMT

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An Application Specific Integrated Circuit for Multi Anode PMT

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***Abstract*— The main purpose of this developpment is to design an "intelligent sensor", composed of one multi anodes PMT, four custom front-end analog chips with embedded analog to digital converter and a pre-processing logical unit. The idea of this design is to improve as most as possible the treatment speed of signals of the PMT. This design must be compact to fit the PMT dimensions, in order to combine them together to form an assembly which will be used in medical imaging research, especially for gamma-ray camera at 144 keV (^{99m}Tc) with NaI(Tl) cristal.**

***Index Terms*— ASIC, Front end electronics, Gamma-ray camera, Intelligent sensor, Mixed signal, PMT.**

I. INTRODUCTION

THIS "intelligent sensor" is designed to fit a 64 anodes PMT. The front-end mixed-signal ASIC contains 16 channels, so 4 chips are necessary to equip the PMT. Each channel consists in an input stage, an integrator, an 8 bits ADC and a shift register. A built-in trigger system allows to start/stop integration and AD conversion. Serial output data are sent to a logical unit (FPGA) which performs a preprocessing, and then, datas are collected on acquisition computer thanks to USB interface (see Fig. 1).

This full custom integrated circuit has been submitted the 5th july 2004. The technology is Austriamicrosystem $0.35\ \mu\mathrm{m}$ CMOS with 4 layers of metal and 2 layers of polysilicon. The total die surface is $9.38\ \mathrm{mm}^2$. Package will be a 52 pins JLCC (J-Leaded Ceramic Carrier).

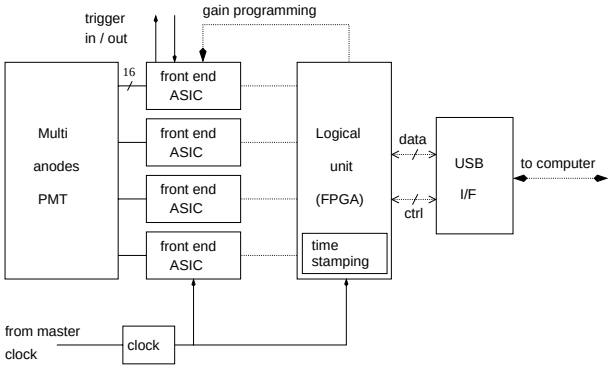

Fig. 1. "Intelligent sensor" overview

II. OVERVIEW

A. Front-end ASIC

The front end ASIC is made of 16 identical channels.

Each channel is made of :

- an input current conveyor (with programmable gain);
- a switched integrator;
- a 8 bits, single ramp analog to digital converter;
- a serial output buffer.

Moreover, it contains an auto trigger with an externally adjustable threshold level and an adjustable integration gate width to synchronize integration and AD conversion.

B. Logical Unit

The logical unit takes place in a Altera Cyclone FPGA. It will ensure :

- fine gain and offset correction;
- time stamping of data;
- front-end input stage gain programming;
- data formatting and USB interface control.

C. USB interface

This is a commercial chip made by FTDI (model 245BM). It ensures a fast and low-cost interface to any recent personal computer. Each sensor has its own link to the acquisition computer.

III. FRONT END ASIC

A. General operation

Each chip input is connected to one anode. The trigger block inside the ASIC performs permanently the sum of the signals of the 16 anodes. When it goes over an externally adjustable threshold, the integration of the current of each anode starts (according to trigger system, others method are described in III-F), thus measuring the charge during an externally adjustable gate. Next, the ADC converter converts the value of the charge of each channel, and finally sends these datas to the external logical unit through the serial output.

B. Input stage

This stage consists in a current conveyor. It converts common mode signal to differential mode, and amplifies signal with a programmable gain.

Digital code	Gain (differential)	Gain (dB)	Bandwidth MHz @ −3 dB)	noise (nA @ bandwidth)
11	2.16	6.7	34	54
01 or 10	3.2	10.1	42	35
00	6.26	15.9	46	30

TABLE I

PERFORMANCE VERSUS GAIN

1) Architecture: This conveyor is made of two identical half stages (Fig. 2), which are cross wired to cancel common mode current : the first half is connected to the anode, and the second half is not connected. The half circuit is made of super common gate input stage (I6 and I7), in which the current is probed with one, two or three transistors (according to the choosen gain – I16 and I5 : only one gain branch is represented). This current is copied with the inverse polarity (I4 and I10 – translation to differential), and copied to output slave transistor. There are two pairs of output transistor : one for the integrator (I2 and I9), and one pair for trigger system (I3 and I8). The power consumption is 500 µA on the 5.5 V and 118 µA on the 2.75 V, *i.e.* about 3 mW per channel (at idle with maximum gain).

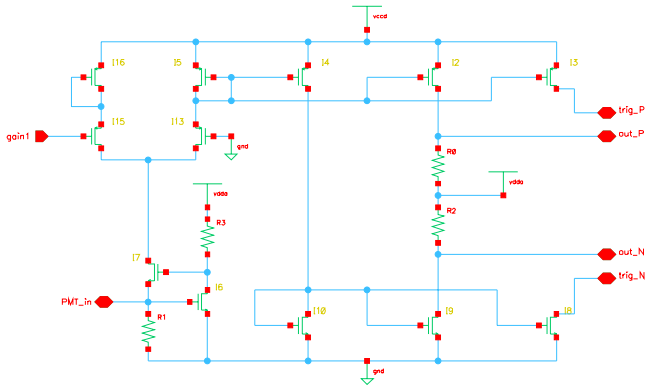

Fig. 2. Half input stage with two gains (simplified)

2) Programmable gain: Three different gains can be programmed (2, 3 or 6) with a 2 bits register. A serial data frame containing the gain of each channel is sent to the chip, according to the clock signal `CK` and the enable signal `EN` (active high). Input `Din` can be chained using the `Dout` output. Each gain is programmed with 2 bits, so 32 bits are necessary to configure all channels.

C. Switched integrator

1) Amplifier: This fully differential amplifier comports a common mode loop to ensure a high CMMR. Simulated characteristics in open loop :
Gain (differential) : 13 570 (82 dB)
Bandwidth : 6.8 kHz
Common mode rejection ratio : 110 dB maximum
Power consumption : 770 µA on the 5.5 V, *i.e* 4.25 mW per channel.

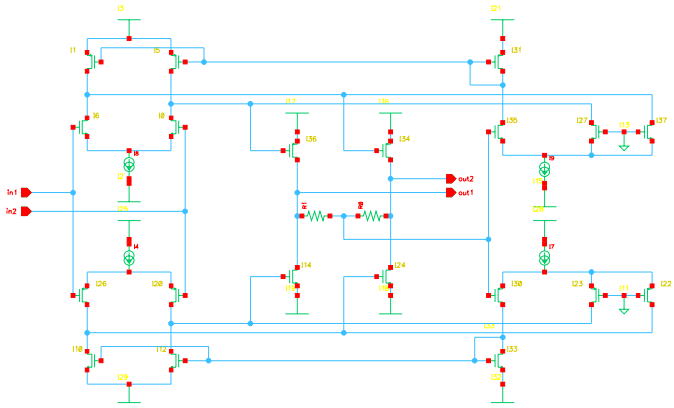

Fig. 3. Amplifier with common mode loop (simplified)

2) Integrator and track & hold: Integrator is made of the amplifier with feedback capacitors. Two pairs of switchs allow to track and integrate the signal, hold the integrated value, and reset the system to begin a new integration. Switches are driven by the trigger system (see III-F). The simulated gain is 129 mV/pC. The output maximum amplitude is 4 V. The linearity is better than 0.07 % @ 3.6 V (28 pC) and is better than 0.25 % of the full scale until 4 V (31 pC).

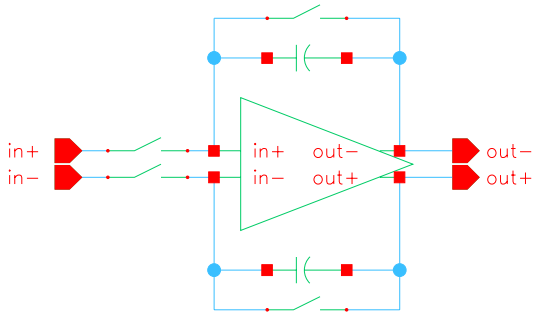

Fig. 4. Integrator and track & hold

D. Analog to digital converter

The analog to digital converter is a 8 bits single ramp ADC (see Fig. 5). The clock frequency is 50 MHz. A constant differential slope (`SC+` and `SC-` – see III-D.2) is generated and compared to the output of integrator. When integrator output is higher than the slope voltage, the counter is stoppped and thus gives the digital value.

1) Comparator: This is a latched comparator which works up to 50 MHz (20 ns). First stage (I10, I0, I7 and I8) is a differential amplifier, loaded by a cascode (I12, I13 I16 and I17). Next comes a shifter (I19 and I20) and the dynamic memory (I23, I24, I25 and I26). The switch is driven by `clk+` and `clk-` signals.
The sensitivity is better than 1.3 mV on the full dynamic of the comparator. The power consumption is 544 µA on the 5.5 V power supply, *i.e.* less than 3 mW per channel.

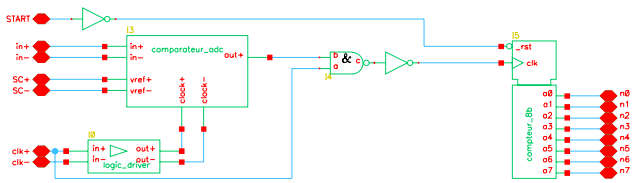

Fig. 5. 8 bits ramp adc

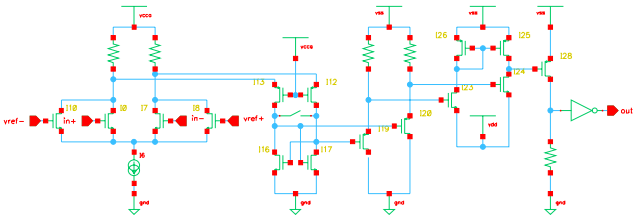

Fig. 6. ADC comparator

2) Slope generator: To generate differential slopes, capacitors are charged with a constant current. We use cascode current source to improve linearity with a large dynamic. The linearity is better than 3.4 mV on the 4 V range of the slope, *i.e.* 0.085 % of the full scale.
The duration of the slope is 5.12 µs : it corresponds to the clock period of the ADC multiplied by 256. The power supply of master transistor of the current source can be externally trimmed, in order to have the right slope, according to clock (`clk+` and `clk-`) period.

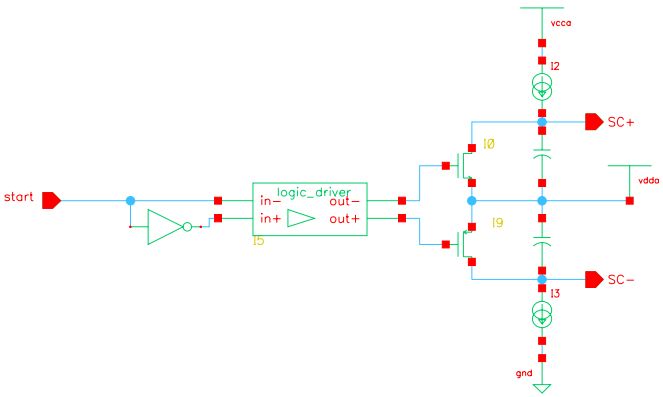

Fig. 7. ADC slope generation

E. Output buffer

After conversion, the result is stored in the 128 bits (1 event : 16x8 bits) output buffer. This buffer automatically sends its contains when the conversion is done (see III-F). The output of this buffer is serial, synchronised with `clk+`/`clk-` differential clocks.

F. Auto trigger

1) Operation: The trigger system allows to begin integration and synchronize ADC and output buffer. Let see Fig. 8. The input resistor sum the current which comes from the 16 channels (`S+`/`S-`). The resulting voltage is compared to external threshold `THR+`/`THR-`. When internal signal goes over threshold, `START` signal becomes high. In the same time, `TRIG_OUT` output becomes high too. This output is usefull to trigger one (or more) other chip : if `TRIG_IN` receives a high level signal, the internal signal `START` becomes high and the acquisition begins. Note that the `TRIG_OUT` output is an open drain output : external resistor is required (500 Ω for example).

As soon as `START` is high, integration begins. The integration gate ranges from 20 to 440 ns according to the voltage on the `GATE_W` pin. Next, analog signal is holded and analog to digital conversion starts. At the end of conversion (when a counter as reach its maximum value), the digital value of each channel is stored in the output buffer and the chip is ready to acquire a new pulse.

2) Data reading: After a pulse is acquired and converted, we have to read its value. This will be done by a FPGA (Field Programmable Gate Array) circuit, which can interface a computer to store and process these data.
The output serial signal is `Sout`. Data are synchronised with `clk+`/`clk-` differential clocks. A rising edge on the `D_VALID` starts the read sequence. `FLAG` at high state at rising edge of `D_VALID` tells that the internal `START` signal has been generated by the internal trigger. `FLAG` at low state indicates that `START` has been set by the `TRIG_IN` input.
The first bit is the most significant bit (MSB) of the 16th channel, and the last bit is the LSB of the 1st channel. An `Sin` input can be used to chain 2 chips.
Fig. 9 shows the output of an event (internal trigger), with the value of the channel #16 wich is ”11000011”.

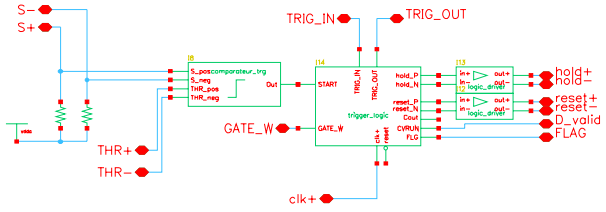

Fig. 8. Trigger overview

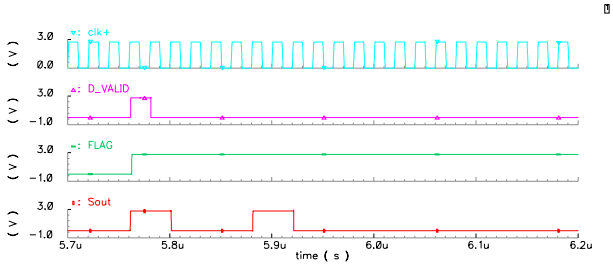

Fig. 9. Example of output (one channel)

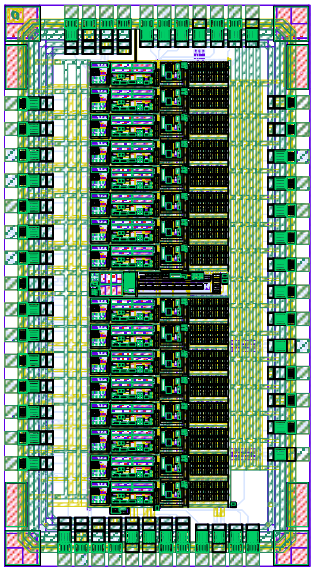

Fig. 10. Layout of front end ASIC

IV. First prototype chip tests

A first chip has been realized in 2003. This prototype is made of one single channel with external controls, and of 4 channels with the built-in trigger. Each channel is made of input stage (without gain selection), the integrator and an output buffer. The functionnalities of the 5 prototypes chip have been extensively tested. Here are summaries of tests results.

A. Single channel test

All synchronisation signals (integration gate and hold) are externaly generated by a pulse generator. On Fig 11, wave #1 is the input pulse (on $50\,\Omega$ charge) the wave #2 is the hold signal, wave #3 is the integration gate and wave #4 is the output signal.

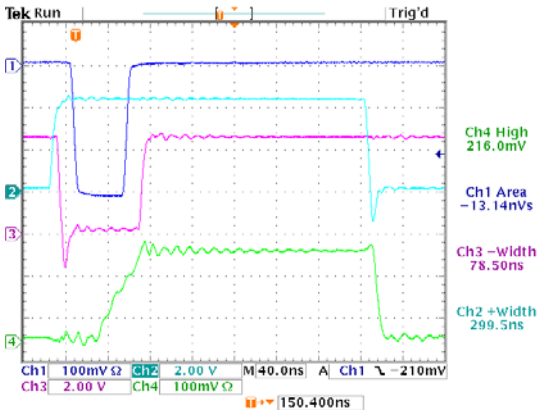

Fig. 11. Oscilloscope capture of single channel test

B. Gain measurements

The simulated value is $129\,\mathrm{mV/pC}$. Fig 12 shows the linearity and the gain of the first channel of 4 chips.

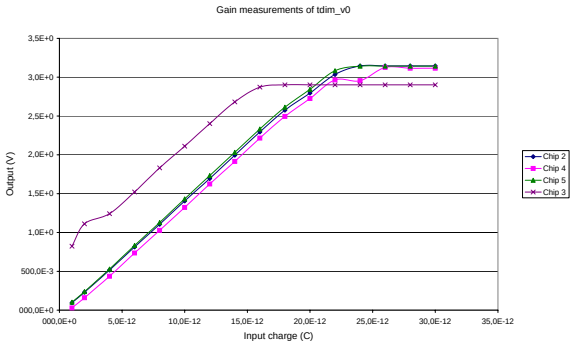

Fig. 12. First protoype linearity

C. Noise

The RMS simulated value of output noise of this first prototype is $2.83\,\mathrm{mV}$ (output). The RMS mean value measured is $2.91\,\mathrm{mV}$. The LSB has a weight of $11.7\,\mathrm{mV}$, so the noise is below the LSB.